a source of gigabit/sec data at said rotary part, said data being subject to jitter;

a slip ring system for transmitting said data from said rotary part to said stationary part, said slip ring system having a rotary slip ring module at said rotary part and a stationary slip ring module at said stationary part;

a first gigabit/sec data link proceeding from said source at said rotary part;

a first clock regenerator connected to said first data link at said rotary slip ring module;

a receiver for said gigabit/sec data at said stationary part;

a second gigabit/sec data link proceeding to said receiver at said stationary part; and

a second clock regenerator connected to said second data link at said stationary slip ring module, said first and second clock regenerators synchronizing said gigabit/sec data, proceeding from said first data link and proceeding to said second data link, to a stable reference clock to prevent said jitter from proceeding from said source to said receiver.

Claim 8 has been amended as follows:

8. (Amended) A data transmission system as claimed in claim 7 wherein each of said parallel clock regenerators calculates a cyclic redundancy check code for each of said packets, and wherein said parallel clock regenerator at said rotary part transmits said cyclic redundancy check code to said source for use in detecting transmission errors in said first data link and wherein said parallel clock regenerator at said stationary part transmits said cyclic redundancy check code to said receiver for use in detecting transmission errors in said second data link.

Claim 18 has been amended as follows:

18.   A method as claimed in claim 17 comprising, at each of said first and second parallel clock regenerators, calculating a [cycling] cyclic redundancy check code for each of said packets, and transmitting the [cycling] cyclic redundancy check code calculated at said first parallel clock regenerator to said source for [minimizing jitter] use in detecting transmission errors in said first data link, and transmitting said [cycling] cyclic redundancy check code from said second parallel clock regenerator to said receiver for [eliminating jitter] use in detecting transmission errors in said second data link.